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Dual-side and three-dimensional microelectrode arrays fabricated from ultra-thin silicon substrates

Jiangang Du[1], **Michael L Roukes**[2] **and Sotiris C Masmanidis**[1]

[1] Department of Computation and Neural Systems, Division of Biology, California Institute of Technology, Pasadena, CA 91125, USA
[2] Kavli Nanoscience Institute, California Institute of Technology, Pasadena, CA 91125, USA

E-mail: sotiris@caltech.edu

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Abstract

A method for fabricating planar implantable microelectrode arrays was demonstrated using a process that relied on ultra-thin silicon substrates, which ranged in thickness from 25 to 50 μm. The challenge of handling these fragile materials was met via a temporary substrate support mechanism. In order to compensate for putative electrical shielding of extracellular neuronal fields, separately addressable electrode arrays were defined on each side of the silicon device. Deep reactive ion etching was employed to create sharp implantable shafts with lengths of up to 5 mm. The devices were flip-chip bonded onto printed circuit boards (PCBs) by means of an anisotropic conductive adhesive film. This scalable assembly technique enabled three-dimensional (3D) integration through formation of stacks of multiple silicon and PCB layers. Simulations and measurements of microelectrode noise appear to suggest that low impedance surfaces, which could be formed by electrodeposition of gold or other materials, are required to ensure an optimal signal-to-noise ratio as well a low level of interchannel crosstalk.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Microfabrication technology promises to significantly enhance the quality of *in vivo* electrophysiological measurements of neuronal activity in terms of spatial resolution, topographical precision and single-cell yield [1, 2]. Microelectromechanical systems (MEMS) offer a high degree of control over electrode position and spacing, and the possibility for integration with electronics [3], drug delivery channels [4], and electrical stimulation sites [5]. MEMS neural probes containing around 100 recording sites have already provided glimpses of the rich dynamics of rodent neurophysiological activity with single cell and spike time accuracy [6]. The design of such probes has primarily focused on providing planar (i.e., two-dimensional, 2D) information. But the immense complexity of neuronal circuitry suggests the development of volumetric (i.e., 3D) electrophysiological recording tools enabling high-resolution measurements of activity within and between multiple cortical regions.

A growing number of different MEMS neural probes have been demonstrated, with a variety of electrode geometries, substrate materials, and methods for fabrication and assembly. Many are inspired by the planar microelectrode architecture [7], which contains multiple electrodes arranged in a single plane, distributed on one or more sharp implantable shafts. An alternative architecture is embodied in the intracortical array [8]. This configuration samples extracellular fields from the tip of each shaft, and though the tips are not confined to a single plane, prospects for dense 3D recording appear limited, as there is only one electrode per shaft. Recent efforts at realizing true 3D recording functionality have begun to show promise [9–12], but the widespread use of those devices appears to remain limited.

This paper presents an alternative method for developing silicon-based neural probes aimed at high single-unit yield, high spatial resolution extracellular measurements. We developed a process for fabricating devices from ultra-thin silicon substrates. Our process shares some similarities

with silicon-on-insulator-based fabrication of neural probes; the thickness of the shafts was defined by the device substrate (25 and 50 μm were demonstrated, although thinner wafers are eventually envisioned), and etching was carried out with deep reactive ion etching (DRIE) [13, 14]. A notable difference in our choice of substrate is that the backside of ultra-thin wafers can be polished and processed in the same manner as the front side. This raises the prospect for increasing device functionality for neuronal recording applications. Our fabrication approach lends itself to high spatial density recordings by offering separately addressable microelectrode arrays on one or both sides of the implanted structure, and a modular assembly scheme for creating multilayer 3D structures. This paper describes the process by which the devices are fabricated and assembled, and also characterizes the capacitive coupling and noise properties of the microelectrodes. The extracellular recording characteristics of such probes have been discussed in a separate publication [15].

The development of dual-side arrays was motivated by the prediction that extracellular fields can be shielded by the neural probe [16], which reduces the probability of detecting action potentials from neurons that are occluded by the shaft. The placement of microelectrodes on both sides of the shaft is thus believed to be a promising solution to this problem. Elimination of shielding effects may lead to increased numbers of recorded single units, which would provide more cell pairs for spike correlation analysis, require fewer experimental sessions, and may ultimately yield more information about neuronal circuitry in the region of study. Double-sided electrode configurations have also been developed as a means of overcoming the shielding problem [17]. However, our dual-side array offers separately addressable sites on the front and the backside, which may provide even better single-unit discrimination. It is finally worth noting that a different type of dual-side probe based on flexible polyimide substrates has been described elsewhere [18].

2. Probe fabrication

2.1. Handling of ultra-thin wafers

In order to avoid fracturing the device wafers, a supporting carrier substrate is used for all critical fabrication steps. The carrier is typically comprised of 500 μm thick Si, Pyrex or quartz. For a majority of processing steps the ultra-thin wafer is temporarily bonded to the carrier by means of a polymeric adhesive (WaferGrip, Dynatex), and debonded by means of a hot solvent (StripAid, Dynatex). The polymeric adhesive is placed between the carrier substrate and the device substrate. In the event of asymmetric stress between the two sides of the device wafer, a small weight is added on top to ensure uniform contact. The stack is then placed in a room-temperature vacuum oven that is allowed to reach 110 °C for 30 min, and then cooled back to room temperature, after which it is ready for processing. The long thermal cycling time ensures the ultra-thin wafer is uniformly adhered to the carrier, which is essential for enabling the subsequent photolithography steps.

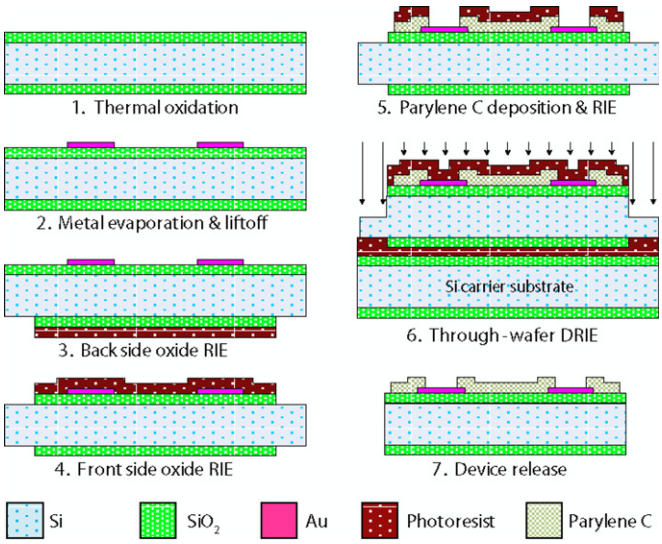

Figure 1. Fabrication process flow for single-side neural probe array built from ultra-thin silicon substrates. Each step relies on the use of a rigid supporting wafer to maintain structural integrity of the device substrate.

In the final DRIE step, the adhesive is replaced with a thin layer of spun-on photoresist (AZ-9245, AZ Electronic Materials), which appears to provide better thermal anchoring to the carrier substrate. After the stack has been made, it is baked at 110 °C for 60 min.

2.2. The single-side device process

The neural recording arrays are manufactured using a series of surface- and bulk-micromachining processing steps, which are illustrated in figure 1. Our single-side devices only contain recording sites on the front side of the wafer, and while these are not as functionally powerful as dual-side arrays, they serve as a useful starting point for describing our fabrication process. We use a double-side polished 50 mm diameter Si (1 0 0) substrate with thickness ranging from 25 to 50 $\pm$ 5 μm (Virginia Semiconductor). The substrates are first thermally oxidized to yield a 2 μm oxide layer on both sides. Next, a negative tone photoresist (nLOF-2035, AZ Electronic Materials) is spun on and patterned to define the metal layer comprising the recording electrodes, interconnects and flip-chip contact pads. Metallization consists of a 30 Å Cr adhesion layer followed by 1500 Å Au. After lifting off the unpatterned metal and photoresist, the wafer is flipped over, remounted on a temporary carrier, and the oxide is selectively removed from the backside using a photoresist mask. This step is vital to obtaining stress-balanced shafts. The wafer is flipped over again to its original orientation, and an RIE step is applied to remove the oxide layer from the front side, forming the shaft profile. A 2 $\pm$ 1 μm parylene C film is then conformally deposited and patterned with an oxygen plasma [19], at which point the insulation layers are fully defined, and the Au recording sites are exposed. For the final DRIE step, a 20 μm thick photoresist film (AZ-9260, AZ Electronic Materials) serves as the masking layer.

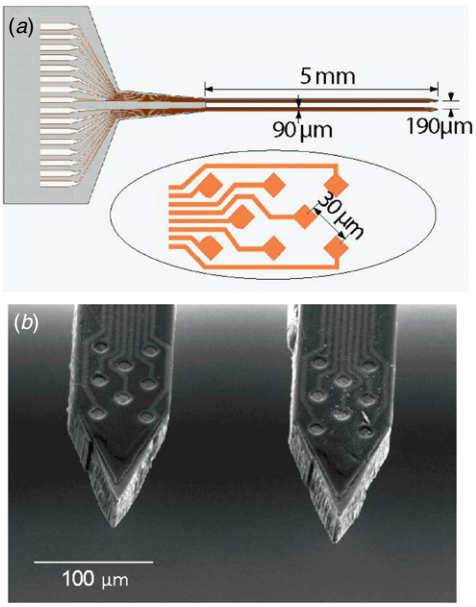

Figure 2. (*a*) Structure of a typical neural probe. This device contains two 5 mm long shafts. The inset shows the recording electrode arrangement. (*b*) SEM image of the tip of a fabricated probe. The gold electrodes have an area of 100 μm^2, and the shafts have a thickness of 50 μm.

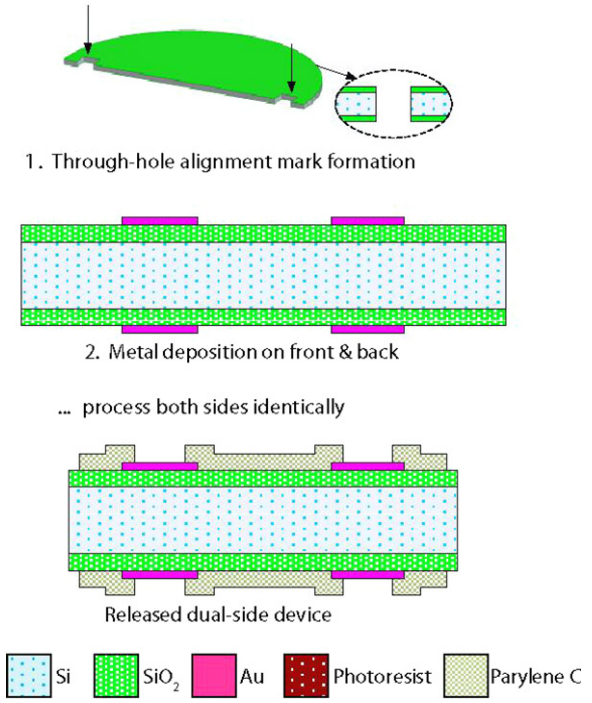

Figure 3. Modified process flow for fabricating dual-side devices on ultra-thin silicon substrates. The etching of through-holes is essential for achieving precise front-to-back feature alignment. Once metal has been evaporated on both sides, the parylene and oxide etch processes are carried out twice before the final DRIE step. The recording sites contain separately addressable leads on each side.

After the etch, the probes are rinsed in acetone, isopropanol and ethanol to remove the photoresist and DRIE residues.

A representative fabricated device is shown in figure 2(*a*), with an expanded SEM view of the tip in figure 2(*b*). This particular array employs 16 recording sites distributed on 2 shafts, which have dimensions of 5 mm $\times$ 90 μm $\times$ 50 μm ($l \times w \times t$), and a horizontal tip spacing of 190 μm. The recording sites have an area of 10 $\times$ 10 μm^2, and are 30 μm apart. Interconnecting wires have a width and separation of 2 μm. As with other planar MEMS neural probes, the array design can be tailored into a plethora of configurations.

2.3. Process modification for dual-side devices

The fabrication of microelectrode arrays on both sides of the device requires precise front-to-back feature alignment. This is realized by etching alignment marks through the ultra-thin wafer at the onset of processing (figure 3). Next we perform metallization, parylene C deposition and insulator etching on both sides using the commonly visible alignment features. As figure 4(*a*) shows, identical arrays are patterned on both sides of the device on the whole-wafer scale. The process yields devices with back-to-front feature alignment better than 10 μm, with 5 μm being the current norm. Importantly, this level of precision could repeatedly not be attained using the optical backside alignment mode of the mask aligner (MA-6, Karl Suss), possibly because of distortions from the carrier substrate used in the handling of ultra-thin wafers. Figures 4(*b*) and (*c*) depict typical front and back views of a dual-side array. Dual-side arrays were successfully fabricated on substrates as thin as 25 μm, as shown in figure 5. The inset of figure 5 is a cross-sectional view of the device, illustrating the vertical side wall produced by the DRIE process.

3. Modular assembly

The finished silicon devices are flip-chip bonded to custom-built flexible polyimide cables or rigid printed circuit boards, which transfer signals to off-chip amplifiers. The modular assembly scheme is represented in figure 6(*a*). The bonds are formed via an anisotropic conductive adhesive film (3M), which upon curing becomes conductive out of plane ($R < 50\ \Omega$) but remains highly resistive in plane ($R > 10^8\ \Omega$). In contrast to wire bonding, flip-chip bonding produces an essentially flat contact area between the neural probe and the printed circuit board (PCB). This enables the connection of PCBs to both sides of the dual-side array, by initially forming contacts on the front side, turning the partially assembled structure over, and bonding with another PCB to the backside contacts. Following assembly, the flip-chip contact region is encapsulated in electronic-grade epoxy. A pair of 16 pin dual in-line packages is used to connect the PCBs to headstage amplifiers.

The same flip-chip bonding process can be applied to create modular 3D arrays consisting of multiple neural probe layers, with interlayer spacing defined by the PCB thickness. Layers are added together by careful manual alignment under a stereo microscope. Multilayer structures are built two modular

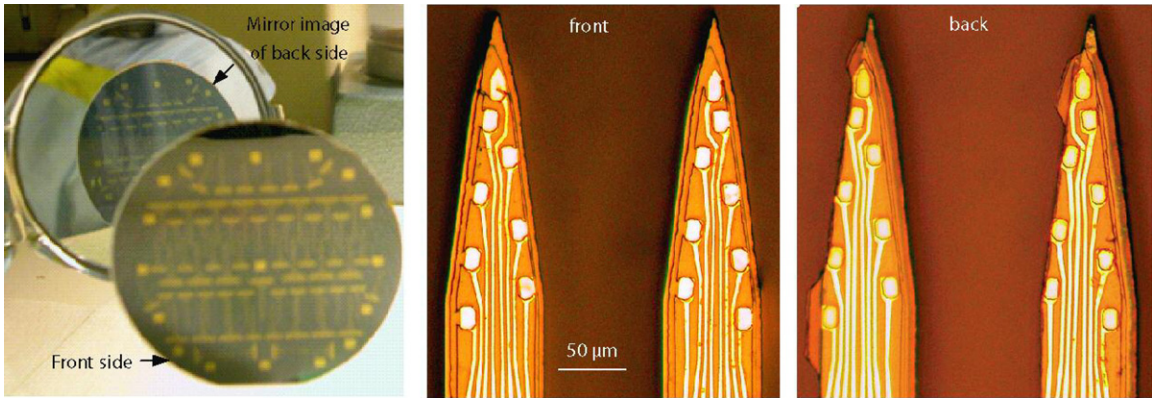

Figure 4. (*a*) The dual-side fabrication process is implemented on a 50 mm wafer. The transparent quartz carrier wafer is not visible. (*b*) Front and (*c*) back views of a representative finished device showing identical patterns. The overhanging structures on the left side of the shafts in (*c*) consist of SiO_2 that is displaced by up to 10 μm from the Si shaft due to slight misalignment of features between the front and backsides.

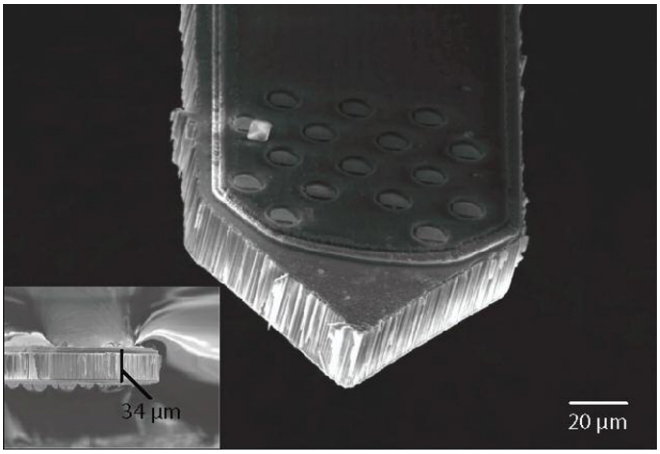

Figure 5. SEM micrograph of the tip of a dual-side neural probe. The total thickness of this structure, indicated by the cross-sectional view in the inset, is 34 ± 1 μm, which includes the ultra-thin substrate (∼28 μm before oxidation, manufacturer's specification = 25 ± 5 μm) and a stack of 2 μm thick thermal oxide and 3 ± 1 μm thick parylene-C film on each side.

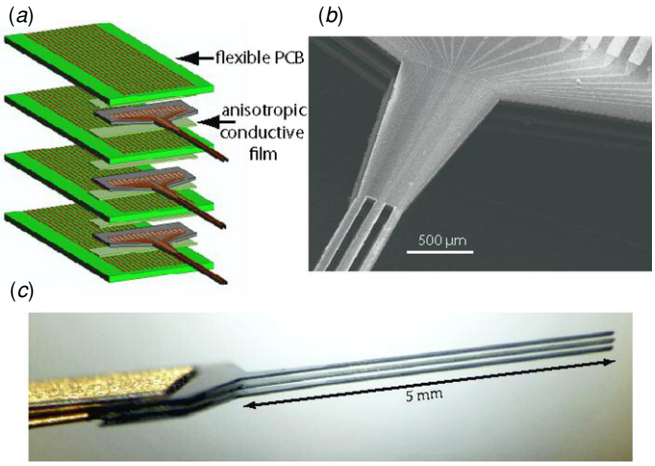

Figure 6. (*a*) Flip-chip assembly scheme for connecting the silicon devices with PCBs. (*b*) SEM micrograph of the rear section of a 50 μm thick shaft array showing the multilayer stacked structure. Adjacent layers have a spacing of 100 μm, which is set by the thickness of the flexible cable. (*c*) Side view of the 50 μm thick shaft array showing that the shafts are stress balanced and are able to retain approximately constant relative spacing.

sections at a time, using the anisotropic conductive film for both device-to-PCB connectivity and as an interlayer adhesive. The SEM image in figure 6(*b*) shows the rear section of a prototype 3 × 3 shaft array (50 μm shaft thickness, 100 μm separation), which contains a total of 144 recording sites (eight electrodes per shaft; two sides). The high degree of stress balance ensures that adjacent layers in the 3D stack retain a constant relative spacing, as illustrated in figure 6(*c*). The flexible cable contains metallic leads on each side, thereby providing separate electrical access to electrodes on the front and back of the silicon probes.

4. Results

4.1. Capacitive coupling effects

Electrical signals in neural probes are susceptible to attenuation from capacitive shunting of the electrodes to the surrounding extracellular fluid [20]. Stray capacitance originates along wiring on the silicon shaft and PCB connecting the recording site to the headstage amplifier, as well as internal capacitance at the headstage. In our devices, these values are, respectively, estimated to be about 3 pF, for a fully inserted probe, and 12 pF. In addition, capacitance between neighboring electrodes (∼1 pF) causes crosstalk between adjacent channels [21]. The amount of attenuation and crosstalk is expected to depend on electrode impedance and signal frequency. In order to gain further insight into capacitive coupling effects, the relationship between impedance and signal attenuation as well as crosstalk was investigated with an analog electronic circuit simulator (SPICE). The equivalent circuit has been depicted in [15]. We assume a purely resistive electrode; this approximation is based on the observation that electrodes have mostly resistive behavior at high frequencies

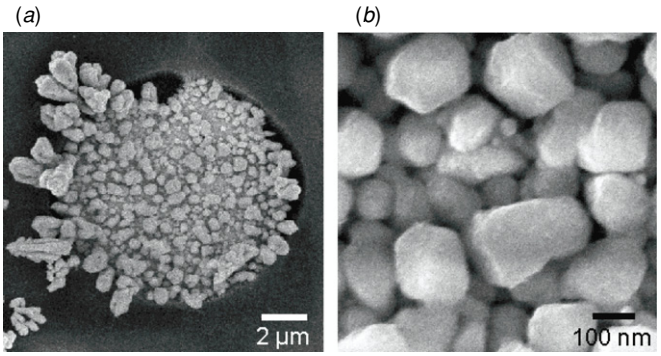

Figure 7. (*a*) Electron micrograph of a gold-electrodeposited microelectrode after a 9 day PBS immersion test. This site had an impedance of 0.65 MΩ on the final day. (*b*) Close-up of the surface of an electrodeposited electrode.

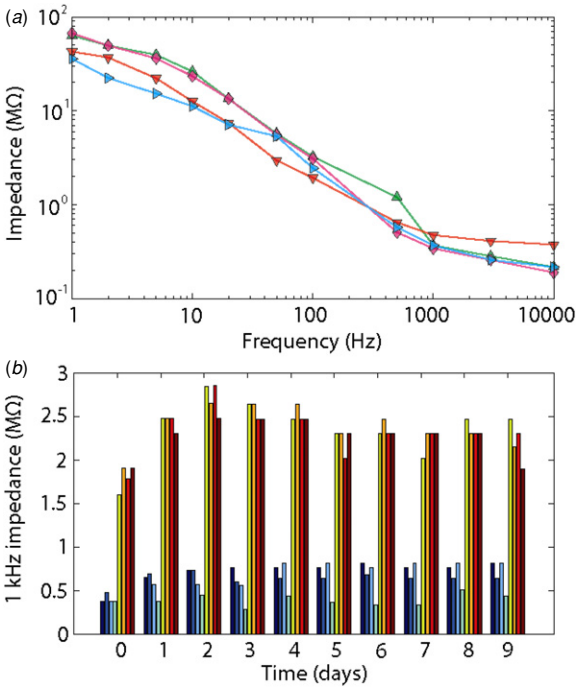

Figure 8. (*a*) Impedance versus frequency of four electrodeposited gold electrodes. (*b*) Electrode impedance measured over the course of 9 days for plated (left half of set) and unplated (right half) recording sites. Uncertainty in measured impedance is ∼5%.

[5], at which the strongest parasitic coupling effects are manifested. The simulations suggest that in order for attenuation and crosstalk to be <2%, the product of impedance and frequency ($Z \cdot f$) must be less than 10^9 Ω Hz. From this relation we predict that ∼1 M Ohm is the maximum impedance that will maintain faithful representations of extracellular signals at 1 kHz. In most recording applications 2% signal attenuation or crosstalk is unlikely to noticeably interfere with the signal analysis. However, increasing the $Z \cdot f$ product tenfold raises the attenuation level to 45% and crosstalk to 10%, which may result in fewer measured spikes, as well as spuriously detected spikes on adjacent channels. While the precise capacitive coupling levels are unique to our devices, PCBs and electronic hardware, the above results can be generalized to any microfabricated neural probe. Integrated electronic components appear to present a promising approach to reducing spurious coupling phenomena [9], although impedance is likely to remain an important design consideration.

4.2. Electrode impedance measurements

Two-terminal impedance measurements were performed in phosphate buffered saline (PBS) solution using an Ag/AgCl reference electrode. A lock-in amplifier (SR-830, Stanford Research Systems) was used to measure current at a predetermined voltage. The current was maintained below 2 nA to avoid excessive ionic transfer effects. The average 1 kHz impedance of untreated 100 μm^2 gold electrodes was found to be 2–3 MΩ, in rough agreement with previously published results [22], and slightly above the capacitive coupling limit discussed in the previous section. We reduced the impedance to less than 1 MΩ by electroplating the surface with gold, the results of which are depicted in figure 7(*a*). This step involved applying brief pulses of current (∼100 ms, 4 μA) in gold plating solution (Sifco), which led to the formation of submicron granular features, as seen in figure 7(*b*). In figure 8(*a*) we plot the impedance spectra of four carefully controlled electrodeposited electrodes. With the exception of some values above 1 kHz, the $Z \cdot f$ product is less than 10^9 ΩHz, which suggests those sites are not strongly susceptible to capacitive shunting and crosstalk effects.

We next examined the stability of electrodes immersed in PBS over a 9 day period. Figure 8(*b*) shows the impedance of four electrodeposited and unplated recording sites, respectively. We find that impedance increased over time for all sites, with the maximum change occurring within the first day. Values appeared to have stopped steadily increasing by the fourth day, although they continued to fluctuate. By the final day of measurement, values had increased by 16–116% relative to the first day. The electrodeposited electrodes remained below 1 MΩ, and were thus expected to continue exhibiting minimal capacitive coupling throughout the 9 day saline immersion.

4.3. Electrode–fluid interface noise

Noise influences a microelectrode's recording quality by limiting its effective range of sight in extracellular space. We performed noise measurements on single- and dual-side devices while they were immersed in PBS. Electrical signals were fed to a custom-built 16-channel headstage and an amplifier (total gain of 2000), whose noise was characterized by shorting its inputs. Figure 9 presents the noise power spectral density (PSD) of two electrodes whose impedances differ by almost an order of magnitude (the lower impedance electrode had an electrodeposited gold surface while the other did not). For comparison, the PSD of a shorted amplifier channel is also shown. Electrode shot noise, which has

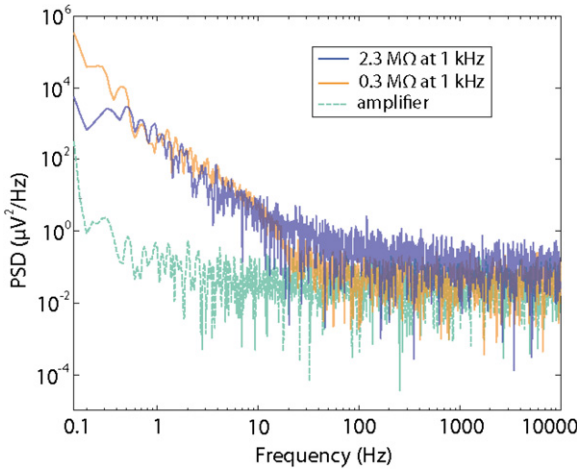

Figure 9. Noise power spectral density (PSD) of two gold microelectrodes (100 μm^2 geometric area) with different impedance values. The lowermost trace represents the noise PSD from the shorted amplifier.

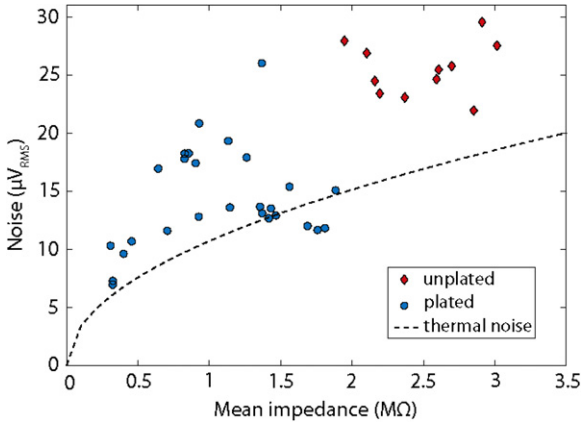

Figure 10. Root-mean-square noise at the electrode–fluid interface as a function of the mean impedance. The measurement bandwidth is 100–7000 Hz, and uncertainty in Z and δV is ∼10% (error bars not shown). Blue circles and red diamonds represent electrodeposited and unplated gold electrodes, respectively. The thermal noise for a resistor with $R = Z$ is also calculated (dashed line).

been attributed to mass and charge transfer at the electrode–fluid interface [23], appears to be the dominant dissipation mechanism below ∼30 Hz.

A different dissipation mechanism, which appears to depend on impedance, dominates at higher frequency. In figure 10, we display the noise in the 100–7000 Hz band as a function of mean electrode impedance, which was adjusted by varying the electrodeposition time. The amplifier background noise has been removed from all data points using mean-square subtraction. In order to calculate the mean impedance value, points on the measured impedance spectrum were interpolated between 100 Hz and 7000 Hz using a cubic spline fit. The area under the impedance–frequency curve was then evaluated, and finally divided by the bandwidth. Noise at the electrode–fluid interface appears to increase with impedance, and in most cases is found to be substantially higher than the thermal dissipation limit. This suggests either additional contributing noise mechanisms [23] or that the electrode's charge transfer resistance is higher than the calculated mean electrode impedance.

The above results clearly point toward the opportunity for avoiding excessive noise and capacitive signal losses by impedance reduction [1]. These observations may help explain why electrodeposited sites often appear to provide superior yield extracellular recordings; another possibility is that the 3D microstructure of plated electrode surfaces is more effective at picking up surrounding extracellular currents. A different obvious path to reducing impedance is to scale up the geometric area of the recording site. It has been predicted that this approach raises the risk for attenuating signals that originate from nearby firing cells [16]. Systematic comparisons of spike shape and amplitude to different geometric and 3D surface electrode areas are needed to address such issues.

5. Conclusions

Ultra-thin ($\leqslant$50 μm) silicon provides an effective platform for the development of multisite implantable neural probes. Despite the challenges of handling such fragile wafers, they appear to offer a unique opportunity to develop high-density arrays with dual-side and 3D recording capabilities. The dual-side array concept has been shown to afford measurement of spiking neurons whose signals would have been electrically shielded beyond the limit of detection by conventional single-side arrays [15]. The development of these recording functionalities is thus important to obtaining a more accurate picture of neuronal activity in the implanted region. Moreover, the quality of extracellular recordings can be substantially degraded by capacitive coupling-mediated signal attenuation and crosstalk, and by noise at the electrode–fluid interface. Proper control of microelectrode impedance is therefore essential to getting the best performance out of such arrays.

The modular assembly method demonstrated here can be scaled up to more complex structures, bringing electrophysiology into the realm of cubic millimeter scale measurements with single cell and spike time resolution. The realization of such a goal raises several challenges related to the front end (i.e., MEMS) development as well in the back end (i.e., electronics) interface that are being addressed in ongoing work.

Acknowledgments

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